

LJTick-RelayDriver

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The LJTick-RelayDriver (LJTRD) is a signal-conditioning module that allows two digital outputs to each control up to 50 volts and 200 mA. The 4-pin design plugs into the standard **DIO/DIO/GND/VS** screw terminal block found on newer LabJacks such as the U3 and UE9.

The pictures below show the LJTRD by itself and plugged in to a LabJack.



Figure 1: LJTick-RelayDriver (LJTRD)



Figure 2: LJTRD With U3

Extending from the back of the LJTRD are four pins. The first two pins provide +5 volt power and ground from the LabJack, although +5 volt power is not used by the LJTRD and thus is not connected to anything. The other two pins connect to digital I/O on the LabJack. The four pins plug directly into the 5.0 mm spaced screw terminals on the LabJack U3/UE9 as shown in Figure 2. The LJTRD should be plugged into a digital I/O block, as opposed to an analog I/O block.

The LJTRD has a 4-position screw-terminal providing the following connections:

RA/RB: The high side of each output switch. When IOA/IOB from the LabJack is set to output-high, the respective switch is closed. When IOA/IOB is set to output-low or input, the respective switch is open. Each switch can hold off up to 50 volts and can sink up to 200 mA.

GNDR: The low side of both output switches. Connected to LabJack GND via a 10 ohm resistor (resistor is on the LJTRD).

VR: Connect the load voltage to this terminal to bias the internal clamping diodes on each switch. If each switch has a different load voltage, the highest voltage should be connected to VR. The clamping diodes help suppress switching transients, and can be particularly important when dealing with inductive loads such as mechanical relays or solenoids. Although this connection is optional, there is usually no reason not to use it.

Following are two figures showing typical connections for the LJTRD. The first diagram shows the general connections, while the second is for the specific case where the LJTRD is controlling VS (5 volts) from the LabJack itself.

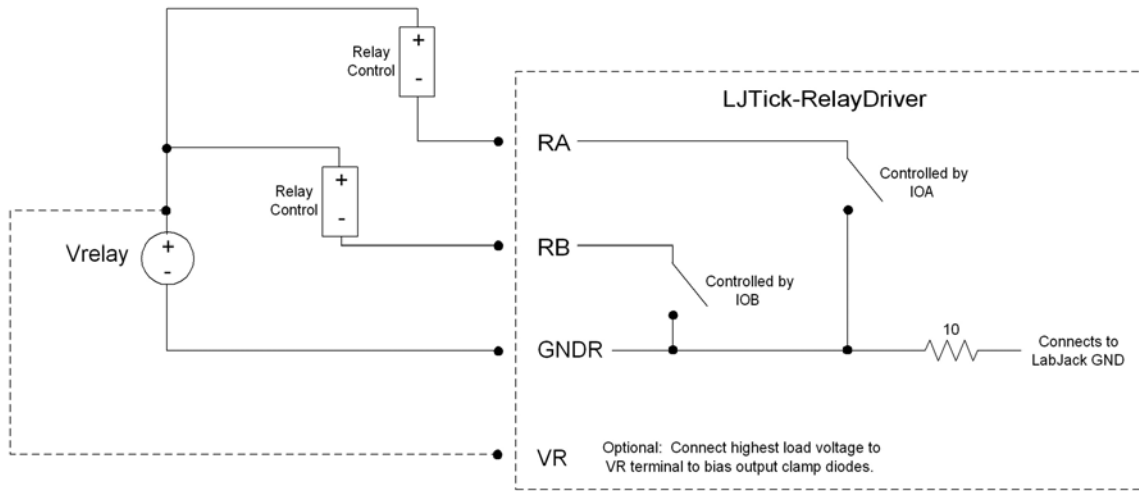


Figure 3: General Connection Diagram

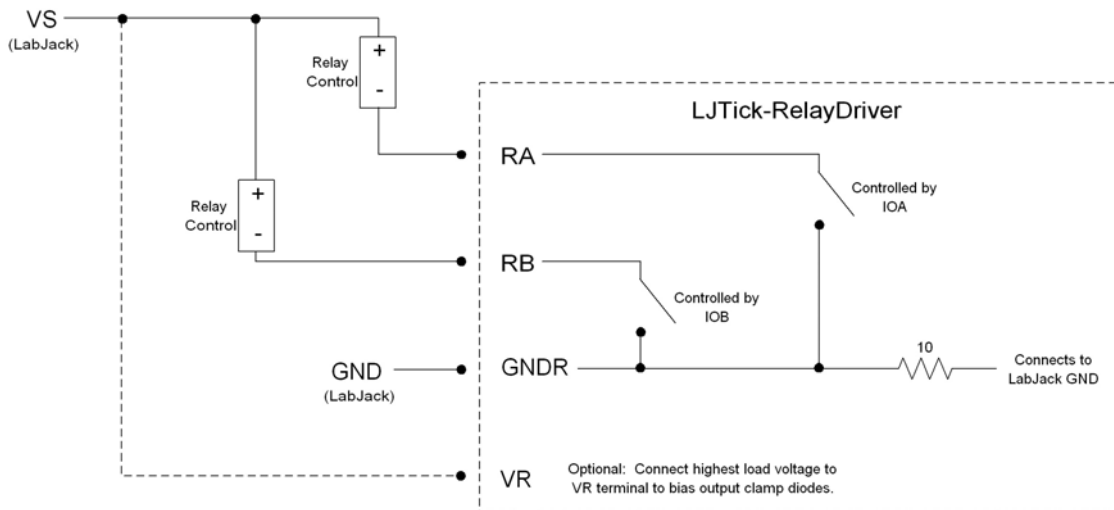


Figure 4: Connection Diagram When Controlling VS from LabJack